UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,757	02/20/2004	Youseff Abdelilah	RPS920030134US1	7394

45211 7590 11/07/2006

KELLY K. KORDZIK
WINSTEAD SECHREST & MINICK PC
PO BOX 50784
DALLAS, TX 75201

EXAMINER	
MOORE, PATRICK M	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 11/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,757	ABDELILAH ET AL.	
	Examiner	Art Unit	
	Patrick M. Moore	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-30 have been examined.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-30 are rejected under 35 U.S.C. 102(b) as being anticipated by So (US Patent # 6,148,389).

a. **As per Claim 1**, So discloses a method for facilitating inter-digital signal processing (DSP) data communications comprising the steps of: reading a first data structure associated **[Figure 21]** with a block of local memory in a first DSP processor core in a complex comprising a plurality of DSP processor cores **[Column 1, Lines 44-50 & Column 2, Lines 29-35]**, wherein said first data structure comprises a first source address indicating a first address of where data is stored in said local memory of said first DSP processor core **[Figure 21 & Column 16, Lines 8-18]**, wherein said first data structure further comprises an indication of a size of a block of memory **["Regions cannot exceed 128KB" of Figure 25]**, wherein said first data structure further comprises a first destination address indicating a second address of where data is to be stored in a local memory of a second DSP processor core **[Figure 21 & Column 16, Lines 8-18]**; and initiating a transfer of moving data said size of said block of memory located

in said first source address in said local memory of said first DSP processor core to said first destination address in said local memory of said second DSP processor core **[Column 13, Lines 1-23]**.

b. **As per Claim 2**, So further discloses the method as recited in claim 1 further comprising the steps of: obtaining a pointer to a second data structure from said first data structure **["Linked List" of Figure 22]**; reading said second data structure, wherein said second data structure comprises a second source address of one of a read pointer and a write pointer, wherein said second data structure further comprises a second destination address of one of said read pointer and said write pointer **[Figure 21 & Column 16, Lines 8-18]**. *As is well known in the art, a linked list, such as the ones disclosed by* **So [Column 23, Lines 8-17]**, *includes data structure entries which point from a preceding structure (e.g. Applicant's claimed "first data structure") to a subsequent structure (e.g. Applicant's claimed "second data structure", "third...", etc.).*

c. **As per Claim 3**, So further discloses the method as recited in claim 2 further comprising the step of: initiating a transfer of said write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core **[Column 13, Lines 1-23]**.

d. **As per Claim 4**, So further discloses the method as recited in claim 2 further comprising the step of: initiating a transfer of said read pointer located in said

second source address in said local memory of said second DSP processor core to said second destination address in said local memory of said first DSP processor core **[Column 13, Lines 1-23]**.

e. **As per Claim 5**, So further discloses the method as recited in claim 2 further comprising the steps of: obtaining a pointer to a third data structure from said second data structure **["Linked List" of Figure 22]**; reading said third data structure, wherein said third data structure comprises a third source address of one of a read pointer and a write pointer, wherein said third data structure further comprises a third destination address of one of said read pointer and said write pointer **[Figure 21 & Column 16, Lines 8-18]**.

f. **As per Claim 6**, So further discloses the method as recited in claim 5 further comprising the steps of: initiating a transfer of said write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core; and initiating a transfer of said read pointer located in said third source address in said local memory of said second DSP processor core to said third destination address in said local memory of said first DSP processor core **[Column 13, Lines 1-23]**.

g. **As per Claim 7**, So further discloses the method as recited in claim 5 further comprising the steps of: initiating a transfer of said write pointer located in said third source address in said local memory of said first DSP processor core to

said third destination address in said local memory of said second DSP processor core; and initiating a transfer of said read pointer located in said second source address in said local memory of said second DSP processor core to said second destination address in said local memory of said first DSP processor core **[Column 13, Lines 1-23]**.

h. **As per Claim 8**, So further discloses the method as recited in claim 2 further comprising the steps of: converting a local address of said write pointer to a global address **[Column 19, Lines 1-11]**; and computing said first source address in said first data structure, wherein said first source address is equal to said size of a block of memory subtracted from said global address of said write pointer **[Figure 24 & Column 23, Lines 1-7 & 23-34]**. *Examiner understands a calculation to find the pointer position of "Region Record N" requires both the "Length" and "Pointer" information of Region Record N-1.*

i. **As per Claim 9**, So further discloses the method as recited in claim 8 further comprising the steps of: reading said local address of said write pointer; and copying said local address of said write pointer into an entry in a third data structure located in said first DSP processor core **[Column 13, Lines 1-23]**.

j. **As per Claim 10**, So further discloses the method as recited in claim 8 further comprising the steps of: reading a local address of said read pointer; and copying said local address of said read pointer into an entry in a third data structure located in said second DSP processor core **[Column 13, Lines 1-23]**.

k. **As per Claim 11**, So discloses a computer program product embodied in a machine readable medium for facilitating inter-digital signal processing (DSP) data communications comprising the programming steps of: reading a first data structure associated **[Figure 21]** with a block of local memory in a first DSP processor core in a complex comprising a plurality of DSP processor cores **[Column 1, Lines 44-50 & Column 2, Lines 29-35]**, wherein said first data structure comprises a first source address indicating a first address of where data is stored in said local memory of said first DSP processor core **[Figure 21 & Column 16, Lines 8-18]**, wherein said first data structure further comprises an indication of a size of a block of memory **["Regions cannot exceed 128KB" of Figure 25]**, wherein said first data structure further comprises a first destination address indicating a second address of where data is to be stored in a local memory of a second DSP processor core **[Figure 21 & Column 16, Lines 8-18]**; and initiating a transfer of moving data said size of said block of memory located in said first source address in said local memory of said first DSP processor core to said first destination address in said local memory of said second DSP processor core **[Column 13, Lines 1-23]**.

l. **As per Claim 12**, So further discloses the computer program product as recited in claim 11 further comprising the programming steps of: obtaining a pointer to a second data structure from said first data structure **["Linked List" of Figure 22]**; reading said second data structure, wherein said second data structure comprises a second source address of one of a read pointer and a write pointer,

wherein said second data structure further comprises a second destination address of one of said read pointer and said write pointer **[Figure 21 & Column 16, Lines 8-18]**.

m. **As per Claim 13**, So further discloses the computer program product as recited in claim 12 further comprising the programming step of: initiating a transfer of said write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core **[Column 13, Lines 1-23]**.

n. **As per Claim 14**, So further discloses the computer program product as recited in claim 12 further comprising the programming step of: initiating a transfer of said read pointer located in said second source address in said local memory of said second DSP processor core to said second destination address in said local memory of said first DSP processor core **[Column 13, Lines 1-23]**.

o. **As per Claim 15**, So further discloses the computer program product as recited in claim 12 further comprising the programming steps of: obtaining a pointer to a third data structure from said second data structure **["Linked List" of Figure 22]**; reading said third data structure, wherein said third data structure comprises a third source address of one of a read pointer and a write pointer, wherein said third data structure further comprises a third destination address of one of said read pointer and said write pointer **[Figure 21 & Column 16, Lines 8-18]**.

p. **As per Claim 16**, So further discloses the computer program product as recited in claim 15 further comprising the programming steps of: initiating a transfer of said write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core; and initiating a transfer of said read pointer located in said third source address in said local memory of said second DSP processor core to said third destination address in said local memory of said first DSP processor core **[Column 13, Lines 1-23]**.

q. **As per Claim 17**, So further discloses the computer program product as recited in claim 15 further comprising the programming steps of: initiating a transfer of said write pointer located in said third source address in said local memory of said first DSP processor core to said third destination address in said local memory of said second DSP processor core; and initiating a transfer of said read pointer located in said second source address in said local memory of said second DSP processor core to said second destination address in said local memory of said first DSP processor core **[Column 13, Lines 1-23]**.

r. **As per Claim 18**, So further discloses the computer program product as recited in claim 12 further comprising the programming steps of: converting a local address of said write pointer to a global address **[Column 19, Lines 1-11]**; and computing said first source address in said first data structure, wherein said first source address is equal to said size of a block of memory subtracted from said

global address of said write pointer **[Figure 24 & Column 23, Lines 1-7 & 23-34]**.

s. **As per Claim 19**, So further discloses the computer program product as recited in claim 18 further comprising the programming steps of: reading said local address of said write pointer; and copying said local address of said write pointer into an entry in a third data structure located in said first DSP processor core **[Column 13, Lines 1-23]**.

t. **As per Claim 20**, So further discloses the computer program product as recited in claim 18 further comprising the steps of: reading a local address of said read pointer; and copying said local address of said read pointer into an entry in a third data structure located in said second DSP processor core **[Column 13, Lines 1-23]**.

u. **As per Claim 21**, So discloses a system, comprising: a plurality of digital signal processing (DSP) units; a direct memory access controller coupled to said plurality of DSP processor cores **[Figure 3, #316]**, wherein said direct memory access controller comprises: a memory unit operable for storing a computer program for facilitating inter-DSP data communications **[Figure 2, #112, #104 & Column 9, Lines 51-62]**; and a processor coupled to said memory unit **[Figure 2, #102 & Column 9, Lines 51-62]**, wherein said processor, responsive to said computer program, comprises: circuitry operable for reading a first data structure associated **[Figure 21]** with a block of local memory in a first DSP processor

core, wherein said first data structure comprises a first source address indicating a first address of where data is stored in said local memory of said first DSP processor core **[Figure 21 & Column 16, Lines 8-18]**, wherein said first data structure further comprises an indication of a size of a block of memory **["Regions cannot exceed 128KB" of Figure 25 and "Length" of Figure 24]**, wherein said first data structure further comprises a first destination address indicating a second address of where data is to be stored in a local memory of a second DSP processor core **[Figure 21 & Column 16, Lines 8-18]**; and circuitry operable for initiating a transfer of moving data said size of said block of memory located in said first source address in said local memory of said first DSP processor core to said first destination address in said local memory of said second DSP processor core **[Column 13, Lines 1-23]**.

v. **As per Claim 22**, So further discloses the system as recited in claim 21, wherein said processor further comprises: circuitry operable for obtaining a pointer to a second data structure from said first data structure **["Linked List" of Figure 22]**; circuitry operable for reading said second data structure, wherein said second data structure comprises a second source address of one of a read pointer and a write pointer, wherein said second data structure further comprises a second destination address of one of said read pointer and said write pointer **[Figure 21 & Column 16, Lines 8-18]**.

w. **As per Claim 23**, So further discloses the system as recited in claim 22, wherein said processor further comprises: circuitry operable for initiating a transfer of said

write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core **[Column 13, Lines 1-23]**.

x. **As per Claim 24**, So further discloses the system as recited in claim 22, wherein said processor further comprises: circuitry operable for initiating a transfer of said read pointer located in said second source address in said local memory of said second DSP processor core to said second destination address in said local memory of said first DSP processor core **[Column 13, Lines 1-23]**.

y. **As per Claim 25**, So further discloses the system as recited in claim 22, wherein said processor further comprises: circuitry operable for obtaining a pointer to a third data structure from said second data structure **["Linked List" of Figure 22]**; circuitry operable for reading said third data structure, wherein said third data structure comprises a third source address of one of a read pointer and a write pointer, wherein said third data structure further comprises a third destination address of one of said read pointer and said write pointer **[Figure 21 & Column 16, Lines 8-18]**.

z. **As per Claim 26**, So further discloses the system as recited in claim 25, wherein said processor further comprises: circuitry operable for initiating a transfer of said write pointer located in said second source address in said local memory of said first DSP processor core to said second destination address in said local memory of said second DSP processor core; and circuitry operable for initiating a transfer

of said read pointer located in said third source address in said local memory of said second DSP processor core to said third destination address in said local memory of said first DSP processor core **[Column 13, Lines 1-23]**.

aa. **As per Claim 27**, So further discloses the method as recited in claim 25, wherein said processor further comprises: circuitry operable for initiating a transfer of said write pointer located in said third source address in said local memory of said first DSP processor core to said third destination address in said local memory of said second DSP processor core; and circuitry operable for initiating a transfer of said read pointer located in said second source address in said local memory of said second DSP processor core to said second destination address in said local memory of said first DSP processor core **[Column 13, Lines 1-23]**.

bb. **As per Claim 28**, So further discloses the system as recited in claim 22, wherein said first DSP processor core comprises: a second memory unit operable for storing a computer program for performing background tasks; and a second processor coupled to said second memory unit, wherein said second processor, responsive to said computer program, comprises: circuitry operable for converting a local address of said write pointer to a global address **[Column 19, Lines 1-11]**; and circuitry operable for computing said first source address in said first data structure, wherein said first source address is equal to said size of a block of memory subtracted from said global address of said write pointer **[Figure 24 & Column 23, Lines 1-7 & 23-34]**.

cc. **As per Claim 29**, So further discloses the system as recited in claim 28, wherein said second processor further comprises: circuitry operable for reading said local address of said write pointer; and circuitry operable for copying said local address of said write pointer into an entry in a third data structure located in said first DSP processor core **[Column 13, Lines 1-23]**.

dd. **As per Claim 30**, So further discloses the system as recited in claim 28, wherein said second DSP processor core comprises: a third memory unit operable for storing a computer program for performing background tasks; and a third processor coupled to said third memory unit, wherein said third processor, responsive to said computer program, comprises: circuitry operable for reading a local address of said read pointer; and circuitry operable for copying said local address of said read pointer into an entry in a third data structure located in said second DSP processor core **[Column 13, Lines 1-23]**.

Response to Arguments

3. Applicant's arguments filed **06 July 2006** have been fully considered but they are not persuasive.

a. As per the arguments directed to the lack of disclosure by **So** of a plurality of DSP processor cores, Examiner notes the express disclosure of "multiple DSP's" as per **Column 1, Line 50**. Examiner understands that such a disclosure clearly anticipates Applicant's claim of a complex comprising a plurality of DSP processing cores.

b. As per the arguments directed to the lack of disclosure for reading a data structure associated with a block of local memory, Examiner notes that **Figure 21** is a depiction of a data structure that is associated with a block of local memory.

c. As per the arguments directed to the lack of a source address, Examiner points out the term "the 128K bytes of read data space (source)" **[Column 16, Lines 9-12]** is a source address and indicates a first address where data is stored, as claimed by Applicant.

d. As per the arguments directed to the lack of disclosure of a data structure in a DSP that indicates the size of a block of memory, Examiner emphasizes that the disclosure in **Figure 25** that "regions cannot exceed 128KB" does indicate a size of a block of memory, as claimed by Applicant.

e. As per the arguments directed to the lack of a destination address, Examiner points out the term "the 128K bytes of read data space (destination)" **[Column 16, Lines 9-12]** is a destination address and indicates a second address where data is stored, as claimed by Applicant

f. As per the arguments directed to the lack of transferring sized data from one DSP to another, **So** expressly discloses how "the DSP can handle the transfer [from source to destination] in lieu of the CPU" in **Column 13, Lines 11-12**.

g. As per the arguments directed towards the lack of a linked list to obtain pointers from a first DSP structure to a second DSP structure, Examiner understands that a linked list points from one member item to the next member item, as is consistent with the definition provided on **Page 14** of Applicant's arguments.

Therefore, such a data arrangement would inherently point from a first data structure (first member) to a second data structure (second member), as is shown by Applicant's provided definition. Additionally, the arguments directed to a lack of a prima facie case of obviousness are moot because the provided definition illustrates how a linked list would inherently anticipate Applicant's claim, as would have been known to one of ordinary skill in the art at the time of invention.

h. As per the arguments directed to the lack of a second data structure with a read and a write pointer, Examiner points out that So discloses such a data structure in **Column 16, Lines 8-18** and understands that multiple such data structure exist in the system taught by **So**.

i. As per the arguments directed to the translation between an address in the DSP space to a PCI address offset, **So** expressly discloses "writing a DSP pointer to a PCI address pointer" and examiner understands that the DSP pointer is exemplary of local address and the PCI address pointer is exemplary of a global address. Such an arrangement must require translation, as claimed by Applicant.

j. As per the arguments directed to the lack of computation of the first source address which is equal to the size of a block of memory subtracted from the global address, Examiner points out **Figure 24** of **So**. Specifically, the illustration that shows the address in question is the size of a 21-bit memory block after

subtracting an 11-bit block from the write pointer, as per **"Region List Structure"** of **Figure 21.b.**

k. As per the arguments directed to the lack of connection between the DMA controller and a plurality of DSP's, Examiner again notes the express disclosure of "multiple DSP's" as per **Column 1, Line 50**.

l. As per the arguments directed to the lack of **So** to disclose all elements in Applicant's **Claim 21**: as illustrated by the citations above, Examiner has shown that **So** discloses all elements and is therefore functionally equivalent to the structure claimed by Applicant.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick M. Moore whose telephone number is (571) 272-1239. The examiner can normally be reached on M-F 9:30AM - 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PMM

HYUNG SOUGH
SUPERVISORY PATENT EXAMINER